CLAIMS

1.- An array of pixels, each pixel comprising:

a pixel element, each pixel element comprising a first pixel electrode for individual control of the pixel element and a second pixel electrode, the second pixel electrode linking substantially all pixel elements in the array and being connected to a common counter-electrode, the first and second pixel electrode forming a first capacitor, the pixel element having a threshold voltage and a modulation voltage,

a pixel refresh circuit, for transferring electric charge related to a pixel data value from a data input of the pixel to the first pixel electrode via a charge transfer path,

a first memory element coupled to the pixel data input for storing electric charge related to the pixel data value,

a first switch element located between the first memory element and the first pixel electrode for controlling charge transfer from the first memory element through the charge transfer path to the first pixel electrode,

wherein the first switch element and the first memory element co-operate to transfer charge related to the pixel data value passively along the charge transfer path to the first capacitor and wherein the array further comprises means for applying a dynamically changing voltage to the common counter-electrode, the dynamically changing voltage changing between a first driving value and a second driving value so that the pixel data value is a signal comprised between zero volts and a data voltage value, the data voltage value being not smaller than the modulation voltage and smaller than the sum of the modulation voltage and the threshold voltage of any of the pixel elements.

2.- An array according to claim 1, wherein the first driving value equals minus the threshold voltage of the pixel elements, and the second driving value equals the sum of the threshold voltage and the modulation voltage of the pixel elements.

3.- An array according to any of the previous claims, the first memory element having a first and a second electrode, the first electrode being coupled to the pixel data input, wherein the second electrode is coupled to ground.

4.- An array according to any previous claim, wherein each pixel further comprises conversion means for converting a stored amount of electric charge related to the pixel data value into a pulse with a pulse width for control of the pixel element, the pulse width corresponding to the stored amount of electric charge.

5.- An array according to claim 4 wherein the conversion means comprises a comparator device.

6.- An array according to claim 5, wherein the comparator device comprises a switching circuit and a wave-shaping circuit.

7.- An array according to claim 6, wherein the switching circuit comprises a resistive load inverter.

8.- An array according to claim 7, wherein the resistive load inverter has a first and a second supply connection for connecting to lower supply voltage and a higher supply voltage respectively, wherein any of the first or second supply connection are connected to a sloping voltage source.

9.- An array according to any of claims 6 to 8, wherein the wave-shaping circuit comprises at least one complementary inverter.

10.- An array according to claim 5, wherein the comparator comprises a shunting resistive device and an inverter.

11.- An array according to claim 10, wherein the shunting resistive device is a resistor.

12.- An array according to claim 10, wherein the shunting resistive device is a transistor with a pulsed gate signal with a low duty ratio.

13.- An array according to claim 10, wherein the shunting resistive device comprises a current mirror.

14.- An array according to any of claims 5 to 14, wherein the comparator comprises at least one current limiting transistor.

15.- An array according to any of claims 4 to 14, wherein the conversion means comprises less than 10 transistors, preferably less than 8

transistors, still more preferred less than 5 transistors.

16.- An array according to any of the previous claims, wherein charge related to the pixel data value when stored in the first memory element generates a data voltage across the first memory element and the passive charge transfer applies substantially the same voltage as the data voltage on the first pixel electrode.

17.- An array according to any of the previous claims, the pixel refresh circuit further comprising:

a mirroring circuit, for losslessly mirroring the pixel data value stored on the first memory element to the first pixel electrode of the pixel element.

18.- An array according to claim 17, wherein the mirroring circuit comprises

a first switch element having a first and a second data electrode and a control electrode, the first switch element being connected with its first data electrode to an electrode of the first memory element and with its second data electrode to the first pixel electrode,

a second memory element for storing data values, the second memory element having a first and a second electrode, the second memory element being connected with its first electrode to the second data electrode of the first switch element, and with its second electrode to the control electrode of the first switch element, and

resetting means, for resetting the data value stored in the second memory element.

19.- An array according to any of the previous claims, furthermore comprising a second switch element between the first memory element and a data line for providing pixel data values.

20.- An array according to any of the previous claims, wherein the pixel element comprises a liquid crystal.

21.- An array according to claim 20, wherein the pixel element comprises an LCOS element.

22.- An array according to any of the previous claims, wherein the first memory element(s) is (are) a storage capacitor(s).

23.- An array according to claim 18 or any claim depending on claim 18,

wherein the second memory element is a storage capacitor.

24.- An array according to any of the previous claims, wherein the first switch element is a transistor.

25.- An array according to any of claims 19 to 24, wherein the second switch element is a transistor.

26.- An array according to any of the previous claims, wherein the array is an active matrix.

27.- A method for refreshing pixel values of an array of pixels, each pixel comprising a pixel element comprising a first pixel electrode for individual control of the pixel element and a second pixel electrode, the second electrode of substantially all pixel elements in the array being connected to a common counter-electrode, the pixel element having a threshold voltage and a modulation voltage, the method comprising passively transferring charge related to pixel data to the first pixel electrode and applying a dynamically changing voltage to the common counter-electrode, the dynamically changing voltage changing between a first driving value and a second driving value so that the pixel data is a signal comprised between zero volts and a data voltage value, the data voltage value being not smaller than the modulation voltage and smaller than the sum of the modulation value and the threshold voltage of any of the pixel elements.

28.- A method according to claim 27, wherein the first driving value equals minus the threshold voltage of the pixel elements, and the second driving value equals the sum of the threshold voltage and the modulation voltage of the pixel elements.

29.- A method according to any of claims 27 or 28, furthermore comprising storing the charge related to pixel data and converting the stored charge into a pulse with a pulse width for control of the pixel element, the pulse width corresponding to amount of stored charge.

30.- A method according to any of claims 27 to 29, wherein the step of passively transferring pixel data comprises losslessly mirroring the data from a first memory element to the first pixel electrode of the pixel element.

31.- A method according to any of claims 27 to 29, wherein the step of passively transferring pixel data comprises transferring the data from either of a set of memory elements over one switch element from a plurality of mutually exclusively driven switch elements.